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CLAIMS

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1. An apparatus comprising:

a processor (i) comprising a number of internal registers and (ii) configured to manipulate contents of said registers in response to instruction codes of a first instruction set; and

5   a translator circuit configured to implement a stack using one or more of the internal registers of said processor.

2. The apparatus according to claim 1, wherein said registers are used to store a top of stack.

3. The apparatus according to claim 2, wherein said top of stack is a Java virtual machine (JVM) top of stack.

4. The apparatus according to claim 1, wherein said internal registers are dynamically allocated in response to stack status.

5. The apparatus according to claim 1, wherein said translator circuit generates one or more instruction codes of the

first instruction set for controlling the internal registers in response to an instruction code of a second instruction set.

6. The apparatus according to claim 5, wherein said instruction code of said second instruction set is a stack instruction.

7. The apparatus according to claim 1, wherein said translator circuit comprises an extension stack.

8. The apparatus according to claim 7, wherein said translator circuit is configured to transfer values between said internal registers and said extension stack.

9. The apparatus according to claim 7, wherein said extension stack is implemented as a last-in first-out (LIFO) memory.

10. The apparatus according to claim 9, wherein said extension stack has both head and tail interfaces.

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11. The apparatus according to claim 7, wherein said extension stack can be emptied/filled to/from a memory device.

12. The apparatus according to claim 11, wherein said memory device comprises a main memory of said processor.

13. The apparatus according to claim 7, wherein said extension stack is configured to indicate an almost empty or almost full condition.

14. The apparatus according to claim 1, wherein said translator circuit comprises a stack management unit configured to track which internal registers are used for the stack.

15. The apparatus according to claim 14, wherein said stack management unit is further configured to track how many internal registers are used for the stack.

16. The apparatus according to claim 14, wherein said stack management unit controls pushes/pops to/from said internal registers.

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17. An apparatus comprising:

means for manipulating data in response to instruction codes of a first instruction set comprising a number of internal registers; and

5   means for using one or more of said internal registers as a top of stack.

18. A method for implementing a Java virtual machine top of stack comprising the steps of:

(A) translating one or more instruction codes of a first instruction set into sequences of instruction codes of a second 5 instruction set; and

(B) manipulating contents of one or more internal registers of a processor in response to said sequence of instruction codes of said second instruction set.

19. The method according to claim 18, wherein said instruction codes of said first instruction set comprise stack operations.

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20. The method according to claim 18 further comprising the step of:

(C) transferring contents of said internal registers to an extension stack or a memory device in response to said sequence

5 of instruction codes of said second instruction set.

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